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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/670,026	09/24/2003	Christopher Philip Ruemmler	200311053-1	4526

22879 7590 11/09/2007

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EXAMINER	
KAWSAR, ABDULLAH AL	
ART UNIT	**PAPER NUMBER**
2195	
MAIL DATE	**DELIVERY MODE**
11/09/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/670,026	RUEMMLER ET AL.	
	Examiner	Art Unit	
	Abdullah-Al Kawsar	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 August 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21 and 26-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 – 21 and 26-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 21 and 26-29 are pending. Claims 22-25 have been canceled.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-4, 6, 8-17, 19, 21 and 26 - 29 are rejected under 35 U.S.C. 103(a) being unpatentable over Williams et al (Williams) US Patent No. 6665750, in view of "Intel Itanium Processor Family Interrupt Architecture Guide"(Intel).

4. As per claim 1, Williams teaches the invention substantially as claim including a method of reducing access latency to a task priority register of a local programmable interrupt controller unit within a microprocessor (col 1, lines 9-12; col 2, lines 55-57), the method comprising:

receiving a command to write an interrupt status value to the interrupt register (Col 4, lines 20 – 21);

writing the interrupt status value to the interrupt register (col 4, lines 20-22); and

writing the interrupt status value into a shadow copy of the interrupt register, wherein the shadow copy is written each time that the interrupt register is written (col 3 lines 12 – 14).

Williams does not teach specifically that the interrupt status value is written into task priority register and the value written is an interrupt mask value.

However, Intel teaches writing the interrupt mask value to the task priority register (Page 2-4 table 2-1, under "TPR=task Priority Register" row; "register Description" --This register support 240 maskable interrupt priority levels--).

It would have been obvious to a person of ordinary skill in art at the time of invention was made to incorporate the teaching of Intel into the method of Williams to write the interrupt mask value in the task priority register. The modification would have been obvious because one of the ordinary skills of the art would have found it motivated to write the interrupt mask value to the task priority register to specify the priority level of the interrupt utilizing the Intel titanium processor family architecture of task priority register.

5. As per claim 2, Williams teaches that receiving a command to read the interrupt mask value from the task priority register (col 2, lines 48 – 49); and

reading the interrupt mask value from the shadow copy, instead of from the task priority register (col 4, lines 34- 36).

6. As per claim 3, Williams teaches that the shadow copy is always written after the task priority register is written (col 5, lines 6 – 11).

7. As per claim 4, Williams teaches that further comprising, upon receiving an interrupt, reading the interrupt mask value from the task priority register and writing the interrupt mask value to the shadow copy (col 4, lines 31- 34).

8. As per claim 6, Williams teaches that the method obviates a need to use a serialize instruction after the task priority register is written because each interrupt performs a serialize operation and performs a read of an interrupt vector register (col 4, lines 31 – 34).

9. As per claim 8, Williams teaches that whereby a latency of reading from the task priority register is substantially reduced (col 4, lines 49 – 51).

10. As per claim 9, Intel teaches that data in the task priority register reflects a level of priority of tasks being performed by the microprocessor (page 2-10, lines 15 – 16).

11. As per claim 10, Intel teaches that the task priority register comprises eight bits to designate up to 256 priority states (page 2-5, lines 1-2; and page 2-10, lines 39-40 through page 2-11, line 1).

12. As per claim 11, Williams that the method is performed by an operating system (col 2, lines 59-61).

13. As per claim 12, Intel teaches that microprocessor further comprising, after writing the interrupt mask to the shadow copy, reading an interrupt vector register at a beginning of an interrupt handler (page 1-4, lines 42-43 through page 1-3, lines 1-3).

14. As per claim 13, Intel teaches that further comprising executing instructions specific to the interrupt handler and returning from the interrupt handler (page 2-15, lines 31-35).

15. As per claim 26, Williams teaches a method of reducing a latency to read a task priority register of a microprocessor (col 2, lines 55-57), the method comprising:

receiving a command to read an interrupt mask value from the task priority register (col 2, lines 48 – 49).

reading the interrupt mask value from the shadow copy at a memory location, instead of from the task priority register itself (col 4 lines 34- 36).

16. As per claim 27, Williams teaches an operating system stored on a computer-readable medium with reduced latency to read a task priority register of a local programmable interrupt controller unit within a microprocessor, the operating system comprising microprocessor-executable code configured read the interrupt mask value from the shadow copy at a memory location, instead of from the task priority register itself (col 3, lines 51 – 56; col 4, lines 34- 36).

17. As per claim 28, Intel teaches the invention substantially including a multiple-processor computer system(page 2-1, figure 2-1) comprising:

a plurality of microprocessors interconnected by a processor bus, wherein each microprocessor includes a task priority register (TPR) with a interrupt mask value for that microprocessor (Page 2-1, fig 2-1; page 2-10, lines 15-16)

Intel does not teach specifically a memory system, including local cache memory on each microprocessor and a main memory, wherein the memory system holds data including an operating system and shadow copies of the TPRs, and wherein the operating system includes executable-code for reading the interrupt mask values from the shadow copies and for maintaining the shadow copies.

However, Williams teaches that a memory system, including local cache memory on each microprocessor and a main memory, wherein the memory system holds data including an operating system and shadow copies of the TPRs, and wherein the operating system includes executable-code for reading the interrupt mask values from the shadow copies and for maintaining the shadow copies (col 3, lines 51 – 56).

18. As per claim 29, Intel teaches the invention substantially including a method of reducing latency to write a task priority register within a microprocessor(page 2-3, lines 33-36)), the method comprising:

upon receiving a command to write an interrupt mask value to the task priority register, writing the interrupt mask value to the task priority register without performing a serialization directly thereafter (page 2-3, lines 37-40; page 2-4, lines 10-19); and

upon receiving an interrupt, performing the serialization and reading an interrupt vector register, wherein a spurious indicator is returned if the interrupt is maskable (page 2-16, lines 1-17).

Intel does not teach specifically that upon receiving an interrupt, performing the serialization and reading an interrupt vector register, wherein a spurious indicator is returned if the interrupt is maskable.

However, Williams teaches that upon receiving an interrupt, performing the serialization and reading an interrupt vector register, wherein a spurious indicator is returned if the interrupt is maskable (col 5, lines 7 – 10, lines 15 – 20)

19. As per claims 14 – 17, 19 and 21, they are computer-readable medium claims of claims 1 – 4, 6 and 8 above. Therefore, they are rejected under the same rational as claims 1 – 4, 6 and 8 above.

20. Claims 5, 7, 18 and 20 are rejected under 35 U.S.C. 103(a) being unpatentable over Williams et al (Williams) US Patent No. 6665750, in view of "Intel Itanium Processor Family Interrupt Architecture Guide"(Intel), and further in view of Demharter (Demharter) US Patent No. 7080205.

21. As per claim 5, Williams and Intel do not teach that if the task priority register is accessed frequently, then the shadow copy is stored in low-latency cache memory within the microprocessor.

However, Demharter teaches that if the task priority register is accessed frequently, then the shadow copy is stored in low-latency cache memory within the microprocessor (col 1 lines 66 – 67).

It would have been obvious to a person of ordinary skill in art at the time of invention was made to incorporate the teaching of Demharter into the combined method of Williams and Intel to store interrupt value in cache memory. The modification would have been obvious because one of the ordinary skills of the art would use cache as interrupt storage for faster access and execution.

22. As per claim 7, Demharter teaches that a latency of writing to the task priority register is substantially reduced (col 2, lines 8 – 10).

23. As per claims 18 and 20, they are computer-readable medium claims of claims 5 and 7 above. Therefore, rejected under the same rational as claims 5 and 7 above.

Response to Argument

24. Applicant's arguments filed 08/30/2007 have been fully considered but they are not persuasive.

25. In the remarks applicant argues that:

(1) Interrupt status value of Williams does not read on the interrupt mask value.

(2) Intel fails to teach writing the interrupt mask value into a shadow copy of the task priority register.

26. Examiner respectfully disagree to applicant:

i. as to points (1) and (2), applicant support his argument with definition of interrupt and interrupt mask value. The rejection is for 103 rejection, Williams teaches writing the interrupt status values in the interrupt register and writing a copy in the system memory wherein Intel teaches writing interrupt mask value in task priority register. It would have been obvious to a person of ordinary skill in art at the time of invention was made to incorporate the teaching of Intel into the method of Williams to write the interrupt mask value in the task priority register. The modification would have been obvious because one of the ordinary skills of the art would have found it motivated to write the interrupt mask value to the task priority register to specify the priority level of the interrupt utilizing the Intel titanium processor family architecture of task priority register (see paragraph 4 above).

Conclusion

27. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

TITLE: Input/output device configured for minimizing I/O read operations by copying values to system memory, US 6,665,750 B1.

TITLE: Arrangement and method for reducing the processing time of a data processing device, US 7,080,205 B2.

TITLE: Multiprocessor computer system with data bus and ordered and out-of-order split data transactions, US 5,191,649.

TITLE: Real time interrupt handling for superscalar processors, US 6,295,574 B1.

TITLE: Interrupt distribution scheme for a computer bus, US 5,282,272.

TITLE: Intel® Itanium® Processor Family Interrupt Architecture Guide, March 2003.

TITLE: The Future of the OS for Internet Applications, Reed Hellman, IEEE, Volume 33 Issue 5 May 2000.

28. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

29. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

30. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abdullah-Al Kawsar whose telephone number is 571-270-3169. The examiner can normally be reached on 7:30am to 5:00pm, EST.

31. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng Ai T. An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

32. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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